



产品规格承认书

Product Specifications for Approval

日欣型号(NISIN Model): NS800FH3001AZ01

客户名称(Customer) :

客户型号(Customer Model): WE380-4G		
Approved by Customer		
结构(Mechanica)	电子(Electronic)	项目 (PM)

日欣光电 (NISIN Optoelectronics)		
Designed	Checked	Approved



R-R-020-A1

修改记录

日期	版本	修改内容	页数	拟制
2024-10-28	V01	初版发行	所有	李世龙

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1.产品规格 (Product Specifications)

面板类型 (Panel Type)	TFT LCD
面板尺寸 (Panel Size)	8 inch
显示类型 (Display Type)	Normal Black
分辨率 (Resolution)	1200 (RGB) x 1920 (dot)
显示点间距 (Dot Pitch)	0.0299 (W) mm × 0.0897 (H) mm
显示色彩 (color)	16.7M
视角 (View Angle)	U/D/L/R: 85/85/85/85
显示驱动IC (Display Driver IC)	HX8279-D01
接口类型 (Interface Type)	MIPI 4 Lane
触摸类型 (TP Type)	外挂 TP
触摸 IC (TP IC)	GT2931
外形尺寸 (Dimensions)	124 (H) X 194.8 (V) X 4.07 (T) (mm)
显示区尺寸 (Display area)	107.64 x 172.22 (mm)
模组亮度 (Module Brightness)	330Cd/m ² (TYP)
触摸屏固件版本	Version: V18

2. 产品图纸 (Product Drawings)

1
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RoHS
HF
REACH

正视图

侧视图

背视弯折图

背视弯折图

J3定义:

NO.	Pin name
1	LED+
2	LED+
3	NC
4	LED-
5	LED-
6	LED-
7	LCD ID1
8	LCD ID2
9	NC
10	NC
11	VDD/3.3V
12	VDD/3.3V
13	RESET/1.8V
14	GND
15	GND
16	GND
17	MIPI DC+
18	MIPI DC-
19	GND
20	MIPI D1+
21	MIPI D1-
22	GND
23	MIPI CLK+
24	MIPI CLK-
25	GND
26	MIPI D2+
27	MIPI D2-
28	GND
29	MIPI D3+
30	MIPI D3-
31	GND

TP技术参数:

- COVER LENS 为强化玻璃(G+G) 康宁基材;
- FPC接口线为IIC标准接口; IO电压:1.8 V;
- IC:GT2931(TX18*RX28);

中断方式: 下拉脉冲; IC是有自动校准的分辨率功能;

- 表面硬度>7H;
- 透光率为86%以上;
- 未注明公差为±0.2mm;
- 产品符合RoHS标准。

NOTES:

- DISPLAY TYPE: 16.7M 8" BOE a-Si LCD
- OPERATING TEMP: -20° C~60° C
- STORAGE TEMP: -30° C~70° C
- MAIN LCD DRIVER:HX8279-D01*2
- BACKLIGHT:8 series and 3 parallel 24
- CHIP-WHITE LED,brightness T.B.D.
- GENERAL TOLERANCE: ±0.2

用0.03mm厚度的黑胶包边处理

PIN TP DEFINITION
1 SHUTDOWN
2 VCC-2.8V
3 SDA-1.8V
4 SCL-1.8V
5 INT-1.8V
6 GND

(CIRCUIT DIAGRAM)
8 series and 3 parallel 24 Pcs Led
VF=21.6V~27.2V, IF=25*3=75mA

J3定义:
1 LED+
2 LED+
3 NC
4 LED-
5 LED-
6 LED-
7 LCD ID1
8 LCD ID2
9 NC
10 NC
11 VDD/3.3V
12 VDD/3.3V
13 RESET/1.8V
14 GND
15 GND
16 GND
17 MIPI DC+
18 MIPI DC-
19 GND
20 MIPI D1+
21 MIPI D1-
22 GND
23 MIPI CLK+
24 MIPI CLK-
25 GND
26 MIPI D2+
27 MIPI D2-
28 GND
29 MIPI D3+
30 MIPI D3-
31 GND

初版

20240926

SHENZHEN NISIN OPTOELECTRONICS CO., LTD

DRAW TYPE : ASSY-Outline

DRAW NO. : NS800FH3001AZ01

Ver. : V00 SCALE : N.T.S.

DRAWN LSL

DATE 20240926

UNIT : mm

CHECKED

DATE

PRO.(3)

APPROVED

DATE

SHEET : 1/1

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3. 接口定义 (The Interface Definition)

PIN	SYMBLE	16	MDSI_DATA3_P
1	NC	17	MDSI_DATA3_N
2	NC	18	GND
3	NC	19	MDSI_DATA2_P
4	LEDA	20	MDSI_DATA2_N
5	LEDK	21	GND
6	VDD (3.3V)	22	MDSI_CLK_P
7	RSTN	23	MDSI_CLK_N
8	FMARK	24	GND
9	GND	25	MDSI_DATA1_P
10	CTP_2V8	26	MDSI_DATA1_N
11	CTP_SDA (1.8V)	27	GND
12	CTP_SCL (1.8V)	28	MDSI_DATA0_P
13	CTP_INT (1.8V)	29	MDSI_DATA0_N
14	CTP_RST (1.8V)	30	GND
15	LCD_ID (1.8V)		

4. 电性特性 (Electrical Characteristics)

4.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Supply power voltage	VDD	-0.30	-	2.1	V
VSP voltage	VSP	-0.30	-	6.60	V
VSN voltage	VSN	-6.60	-	0.30	V
VPP (OTP power)	VPP	-	-	9.0	V
VGH voltage	VGH	-0.30	-	VGL+32V	V
VGL voltage	VGL	VGH-32V	-	0.30	V
Operating Temperature	T _{OPR}	-20	-	+85	°C
Storage temperature	T _{STG}	-55	-	125	°C

4.2 Typical operating condition

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Supply power voltage	VDD	1.7	1.8	2.0	V
VSP voltage	VSP	4.5	-	6.0	V
VSN voltage	VSN	-4.5	-	-6.0	V
VGH voltage(external VGH)	VGH_EXT	8.7	-	20	V
VGL voltage(external VGL)	VGL_EXT	-18	-	-6.7	V
VGH voltage(internal VGH)	VGH_INT	8.7	-	18	V
VGL voltage(internal VGL)	VGL_INT	-16	-	-6.7	V
VPP (OTP power)	VPP	8.0	8.25	8.5	V

43 DC electrical characteristics

(Test condition: VDD=1.7~2.0V, T_{OPR} =-20°C~+85°C, VSS=VSSA=VSS IF=0V)

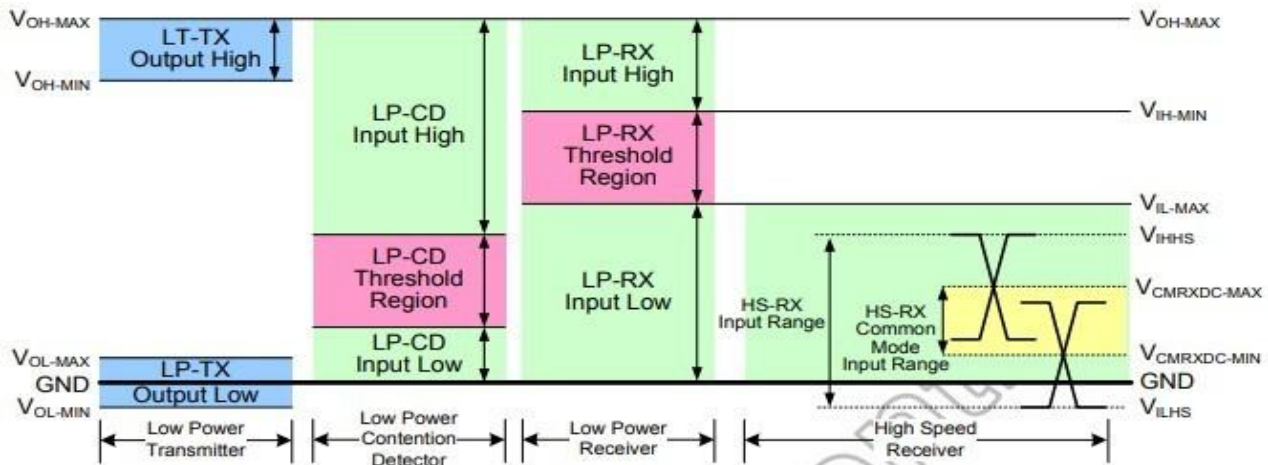
Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
VDD input high level voltage	VIH1	0.8 x VDD	-	VDD	V	-
VDD input low level voltage	VIL1	VSS	-	0.2 x VDD	V	-
VCC input high level voltage	VIH2	0.8 x VCC	-	VCC	V	-
VCC input low level voltage	VIL2	VSS	-	0.2 x VCC	V	-
Input leakage current	IL1	-1	-	+1	μA	-
SDAO output high level voltage	VOH	0.8 x VDD	-	VDD	V	-
SDAO output low level voltage	VOL	VSS	-	0.2 x VDD	V	-
VLP output voltage	VLP	1.1	1.2	1.4	V	I _(VLP) <10mA
VCL output voltage	VCL	-2.1	-2.4	-3.00	V	I _(VCL) <60mA
VGH output voltage	VGH	8.7	-	18	V	I _(VGH) <5mA
VGL output voltage	VGL	-16	-	-6.7	V	I _(VGL) <5mA
VGPH output voltage	VGPH	4.0	4.5	5.5	V	-
VGPL output voltage	VGPL	0.1	0.2	1.6	V	-
VGNH output voltage	VGNH	-5.5	-4.5	-4.0	V	-
VGNL output voltage	VGNL	-1.6	-0.2	-0.1	V	-
Driving current of GOUT outputs	IGOS	1	-	-	mA	GOUT1~20 VO=15V vs 14.7V VGH=15V,VGL=-13V
Sinking current of GOUT outputs	IGOD	1	-	-	mA	GOUT1~20 VO=-13V vs -12.7V VGH=15V,VGL=-13V
VCOM output voltage	VCOM	-2.75	-	-0.20	V	-
Input terminal pull-high resistance	RPU	-	300	-	KΩ	VDD=1.8V
Input terminal pull-low resistance	RPD	-	300	-	KΩ	
Source output level deviation	Gray code= 0 ~ 14	-	-	40	mV	-
	Gray code= 241 ~ 255	-	-	40	mV	
	Gray code= 15 ~ 31	-	-	30	mV	
	Gray code= 208 ~ 240	-	-	20	mV	
Source output offset deviation	Gray code= 0 ~ 14	-	-	50	mV	-
	Gray code= 241 ~ 255	-	-	50	mV	
	Gray code= 15 ~ 31	-	-	40	mV	
	Gray code= 208 ~ 240	-	-	30	mV	
Withstanding current capability	IVDD capability	-	-	40	mA	-
	IVSP capability	-	-	50		
	IVSN capability	-	-	-50		
VSP current consumption	Standby mode	I _{vsps}	-	1.2	mA	Note ⁽²⁾
	ULPS mode	I _{vspu}	-	6	μA	Note ⁽³⁾
VSN current consumption	Standby mode	I _{vsns}	-	-0.15	mA	Note ⁽²⁾
	ULPS mode	I _{vsnu}	-	-12	μA	Note ⁽³⁾
VDD current consumption	Normal mode	I _{vdd}	-	30	mA	Note ⁽¹⁾
	Standby mode	I _{vdds}	-	1.1	mA	Note ⁽²⁾
	ULPS mode	I _{vddu}	-	150	μA	Note ⁽³⁾
VPP operation current	I _{vpp}	-	-	8	mA	-

Note: (1) Condition: one chip current, VDD=1.8V, 25°C, 1200RGBx1920 resolution, MIPI frequency 950mbps, frame rate 60Hz, all setting are default.

(2) Condition: one chip current, VDD=1.8V, 25°C, all function and MIPI input stop. And let MIPI input state keep ULPS to reduce more current consumption in standby mode.

(3) Condition: one chip current, VDD=1.8V, VSP=5.5V, VSN=-5.5V 25°C

44 MIPI DC characteristics



DC characteristics for MIPI LP mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Logic 1 input voltage	V_{IH}	880	-	-	mV
Logic 0 input voltage	V_{IL}	0	-	550	mV
Logic 1 output voltage	V_{OH}	1.1	1.2	1.3	V
Logic 0 output voltage	V_{OL}	-50	-	50	mV

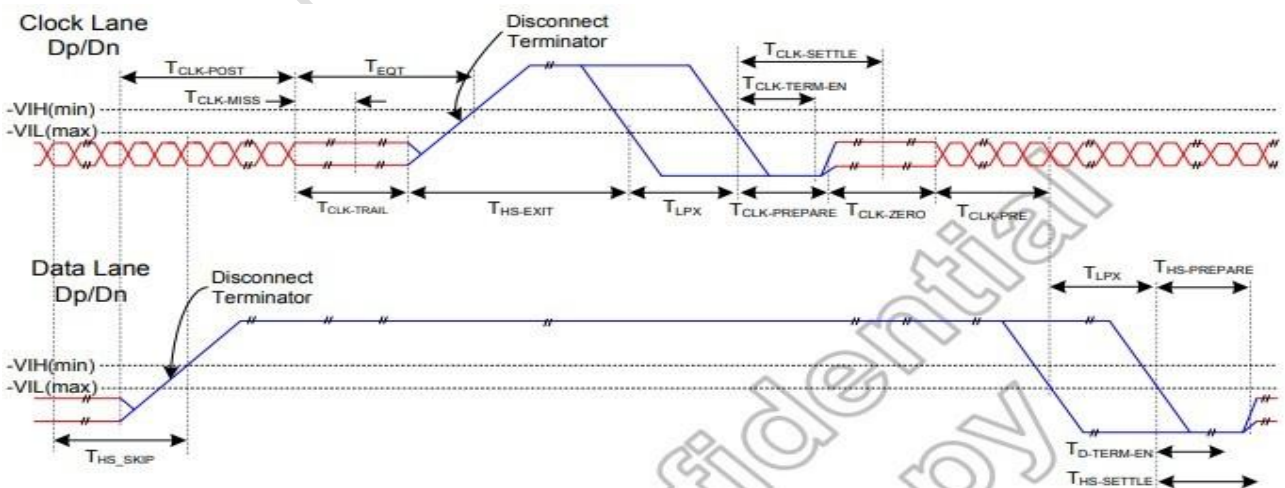
DC characteristics for MIPI HS mode

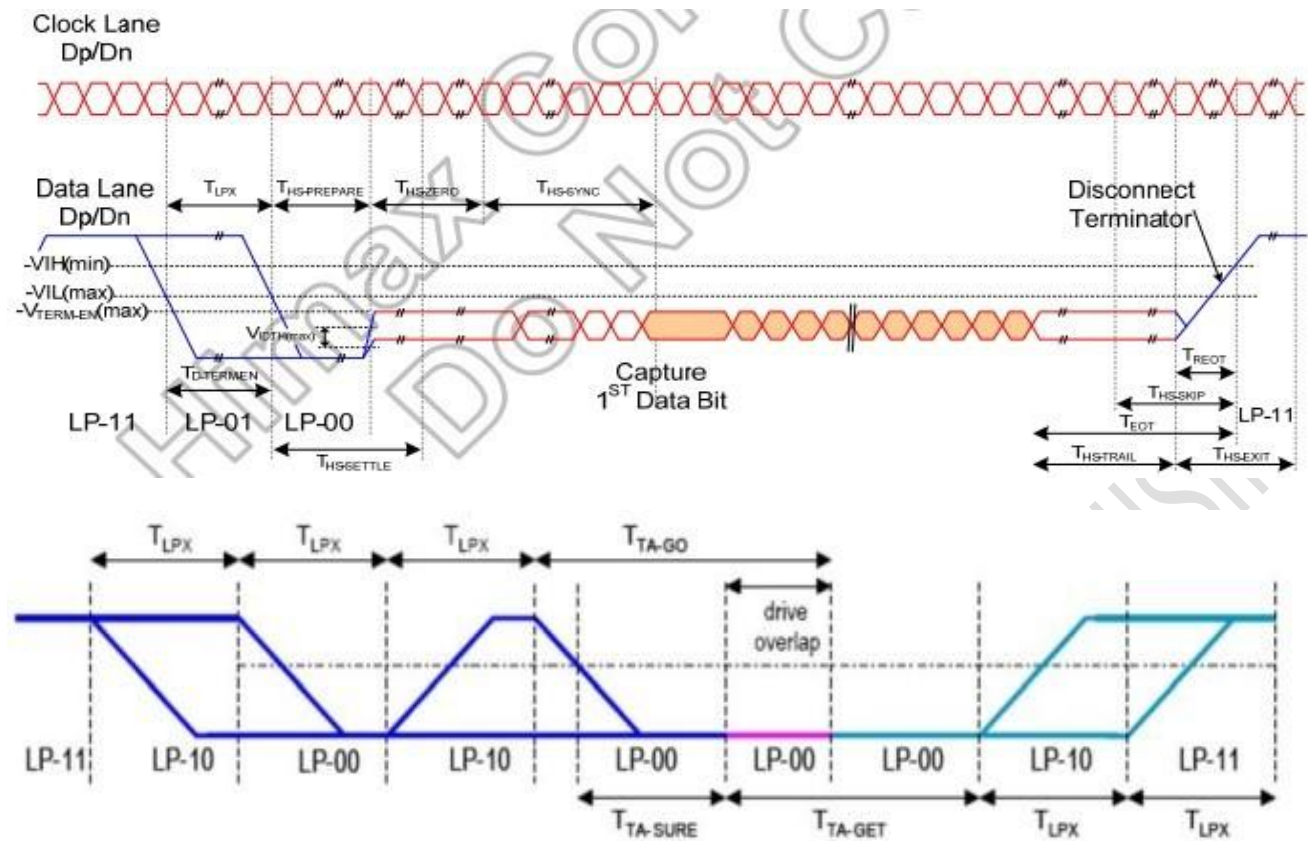
Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Common-mode voltage HS Receive mode	V_{CMRXDC}	70	-	330	mV
Differential input high threshold ⁽¹⁾	V_{IDTH}	-	-	70	mV
Differential input low threshold ⁽¹⁾	V_{IDTL}	-70	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Differential input impedance	Z_{ID}	80	100	125	Ω
HS transmit differential voltage (VDP-VDN)	$ VOD $	140	200	270	mV

Note: (1) V_{IDTH} and V_{IDTL} only for reference, related to power and ground noise, this spec need to check on panel performance to fine tune

45 AC CHARACTERISTICS

4.5.1. MIPI AC characteristics





4.5.2 DPHY Clock transmission & HSDT Bursts

MIPI AC Characteristics

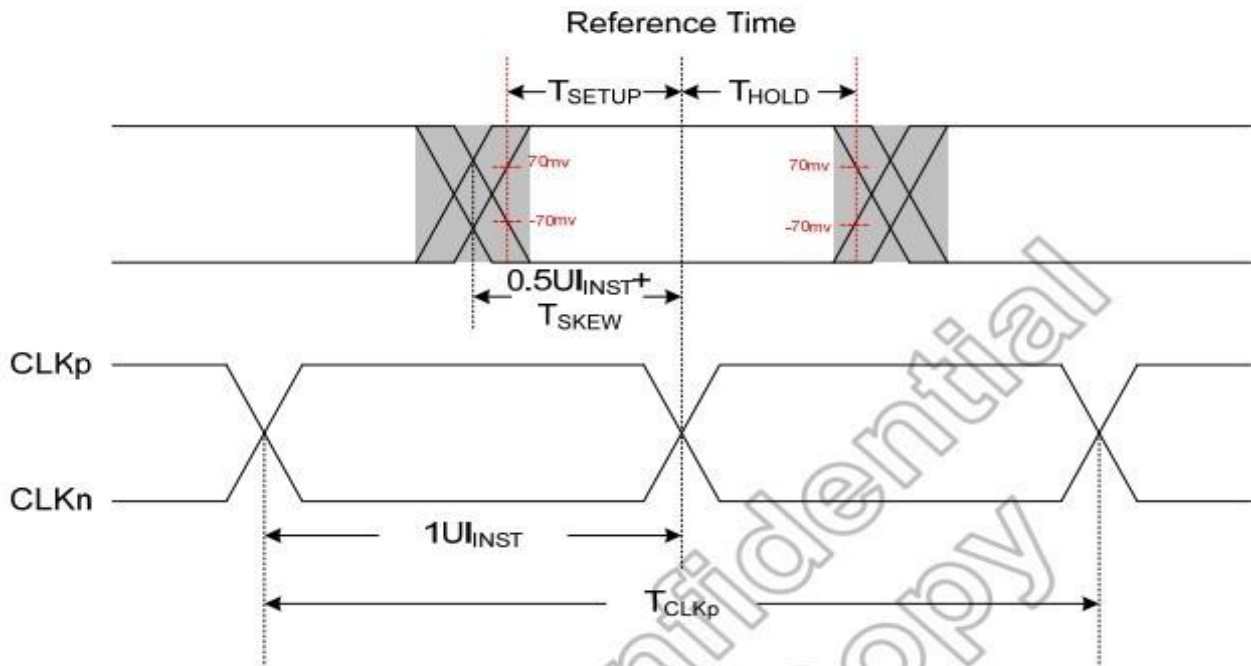
Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
T _{REOT}	30%-85% rise time and fall time	-	-	35	ns
T _{CLK-MISS}	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
T _{CLK-POST} *1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of T _{HS-TRAIL} to the beginning of T _{CLK-TRAIL} .	60 ns + 52*UI (For DCS)	-	-	ns
T _{CLK-PRE}	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	ns
T _{CLK-SETTLE}	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of T _{CLK-PRE} .	95	-	300	ns
T _{CLK-TERM-EN}	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses V _{IL,MAX} .	-	-	38	ns
T _{HS-SETTLE}	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of T _{HS-PREPARE} .	85 ns + 6*UI	-	145 ns + 10*UI	ns
T _{EOT}	Time from start of T _{HS-TRAIL} or T _{CLK-TRAIL} period to start of LP-11 state	-	-	105ns+48*UI	-
T _{HS-EXIT} (1)	time to drive LP-11 after HS burst	100	-	-	ns
T _{HS-PREPARE}	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
T _{HS-PREPARE} + T _{HS-ZERO}	T _{HS-PREPARE} + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
T _{HS-SKIP}	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
T _{HS-TRAIL}	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T _{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T _{LPX}	Ratio of T _{LPX(MASTER)} /T _{LPX(SLAVE)} between Master and Slave side	2/3	-	3/2	-
T _{TA-GET}	Time to drive LP-00 by new TX	-	5*T _{LPX}	-	ns
T _{TA-GO}	Time to drive LP-00 after Turnaround Request	-	4*T _{LPX}	-	ns
T _{TA-SURE}	Time-out before new TX side starts driving	T _{LPX}	-	2*T _{LPX}	ns

Note: (1) For image transmission:

T_{CLK-POST} min value = 164 when MIPI max frequency per lane = 0.53Gbps.

T_{CLK-POST} min value = 112 when MIPI max frequency per lane = 1Gbps

4.5.3 MIPI data-clock timing specification



Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
UI instantaneous	UI_{INST}	1.0	-	12.5 ⁽¹⁾	ns
Data to clock setup time	T_{SETUP}	0.15	-	-	UI_{INST}
Data to clock hold time	T_{HOLD}	0.15	-	-	UI_{INST}

Note: (1) This value corresponds to a minimum 80 Mbps data rate.

4.5.4 Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of low can be shown as the following.

(VDD=1.7V~2.0V, VSS=0V, T_{OPR} = -20°C~+85°C)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Reset low pulse width	$Trst$	-	20	-	-	μ S

Table 13.5: Reset timing

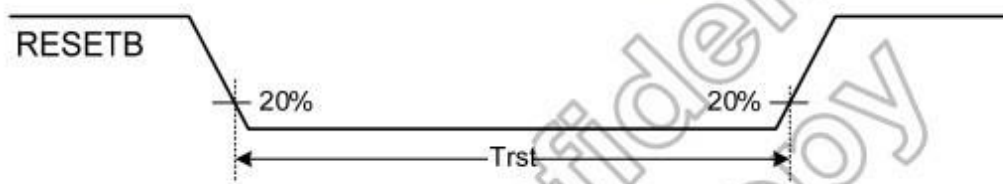
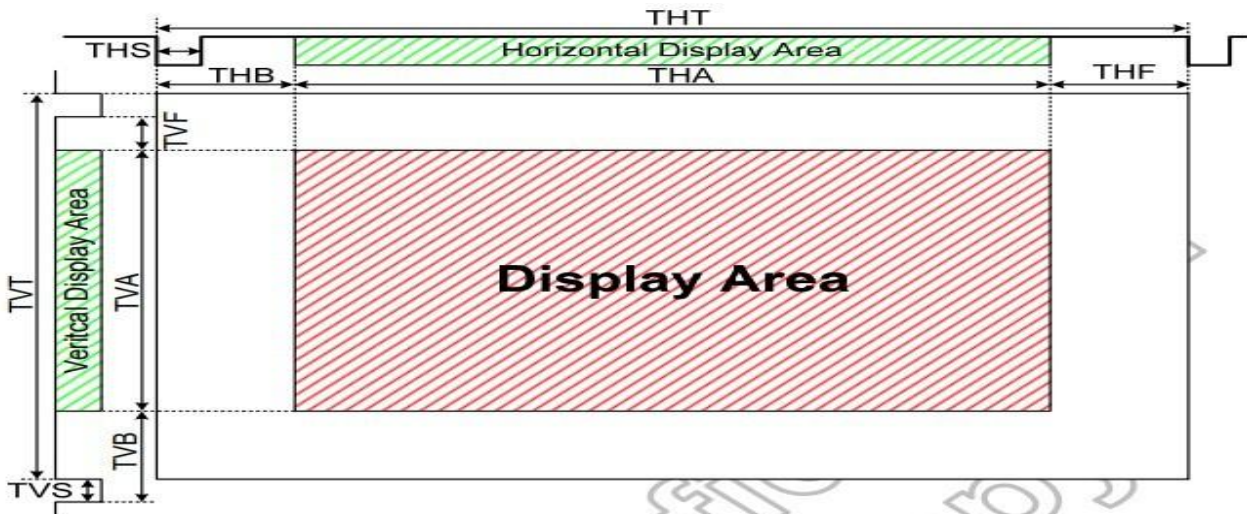
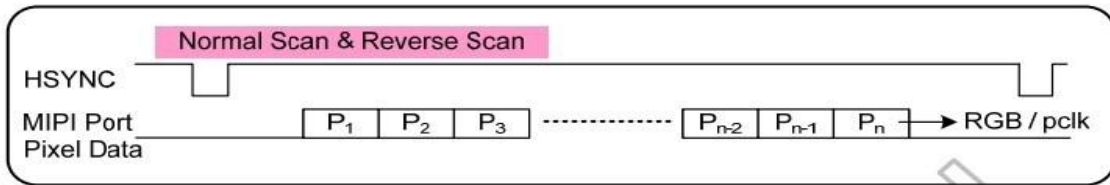


Figure 13.6: Reset timing

46 MIPI Video input timing



MIPI Multi-Drop type when normal or reverse scan.



Input Timing	Symbol	1200RGBx1920			1200RGBx1600			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
PCLK Frequency	-	-	156	-	-	131	-	MHz
Horizontal Total	THT	1270	1340	2047	1270	1340	2047	DCLK
Horizontal Synchronization	THS	10	24	-	10	24	-	DCLK
Horizontal Back Porch	THB ⁽¹⁾	50	80	-	50	80	-	DCLK
Horizontal Address	THA	-	1200	-	-	1200	-	DCLK
Horizontal Front Porch	THF	20	60	-	20	60	-	DCLK
Vertical Frequency	-	-	60	-	-	60	-	Hz
Vertical Total ⁽²⁾	TVT	⁽³⁾	1944	2047	⁽³⁾	1624	1750	THT
Vertical Synchronization	TVS	⁽³⁾	2	-	⁽³⁾	2	-	THT
Vertical Back Porch	TVB	⁽³⁾	10	-	⁽³⁾	10	-	THT
Vertical Address	TVA	⁽³⁾	1920	-	⁽³⁾	1600	-	THT
Vertical Front Porch	TVF	⁽³⁾	14	-	⁽³⁾	14	-	THT

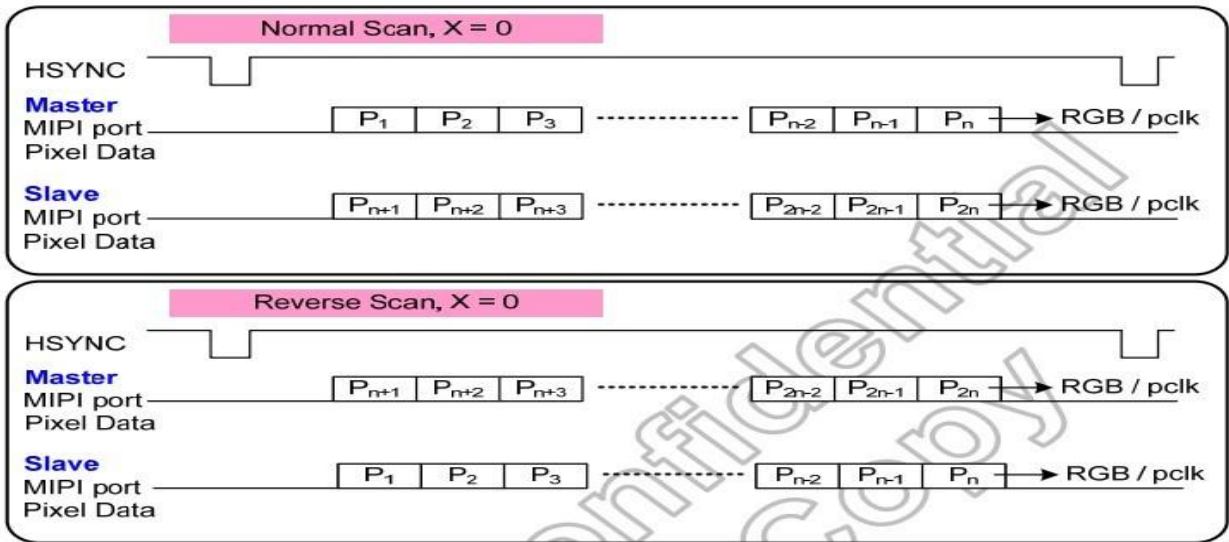
Input Timing	Symbol	1080RGBx1920			600RGBx1024			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
PCLK Frequency	-	-	142	-	-	48	-	MHz
Horizontal Total	THT	1150	1220	2047	670	760	1200	DCLK
Horizontal Synchronization	THS	10	24	-	10	24	-	DCLK
Horizontal Back Porch	THB ⁽¹⁾	50	80	-	50	80	-	DCLK
Horizontal Address	THA	-	1080	-	-	600	-	DCLK
Horizontal Front Porch	THF	20	60	-	20	80	-	DCLK
Vertical Frequency	-	-	60	-	-	60	-	Hz
Vertical Total ⁽²⁾	TVT	⁽³⁾	1944	2047	⁽³⁾	1056	1176	THT
Vertical Synchronization	TVS	⁽³⁾	2	-	⁽³⁾	2	-	THT
Vertical Back Porch	TVB	⁽³⁾	10	-	⁽³⁾	10	-	THT
Vertical Address	TVA	⁽³⁾	1920	-	⁽³⁾	1024	-	THT
Vertical Front Porch	TVF	⁽³⁾	14	-	⁽³⁾	22	-	THT

Note: (1) THB includes THS.

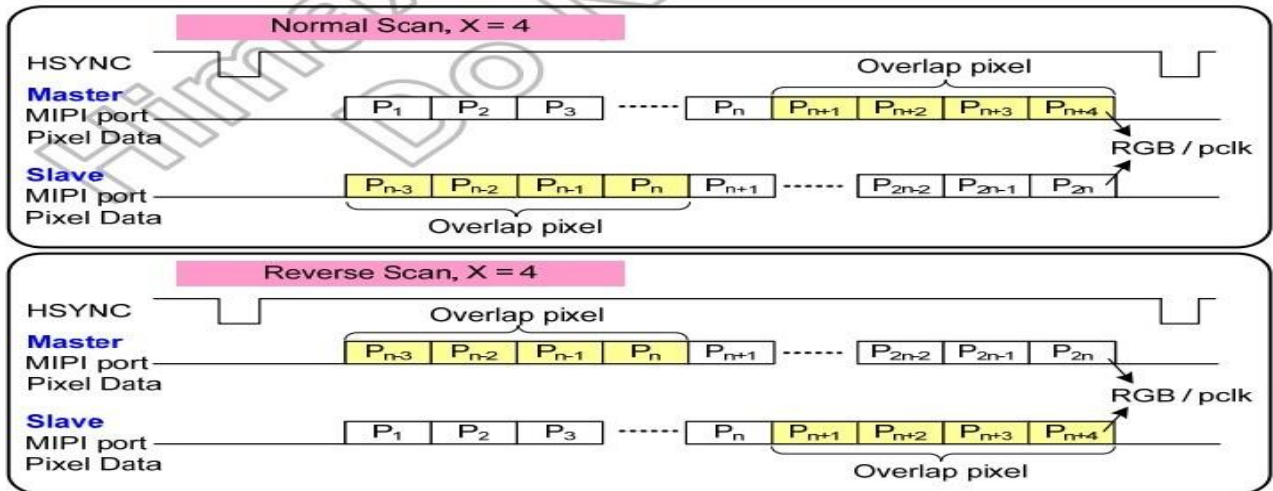
(2) (Vertical frequency) x THTxTVTx24bits → total operation bandwidth.

(3) The min. value of Vertical porch is depending on GOA timing. Please refers to the AP. Note for the min value.

MIPI R/L type timing when normal and reverse scan. Below figure is no overlap X=0 between left and right display data. The value of X can be setting by page0 0xB7[2:1].

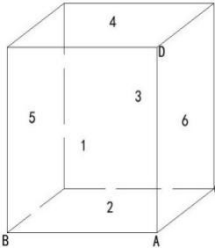


At MIPI R/L type, it supports overlap X= 2,4 between left and right display data. Below figure is example for overlap X=4. The value of X can be setting by REG OVERLAP (page0 0xB7[2:1]). **The overlap pixel must be sent in the zigzag panel application.**



Input Timing	Symbol	1200RGBx1920			1200RGBx1600			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
PCLK Frequency	-	-	86	-	-	72	-	MHz
Horizontal Total	THT	670	740	1200	670	740	1200	DCLK
Horizontal Synchronization	THS	10	24	-	10	24	-	DCLK
Horizontal Back Porch	THB ⁽¹⁾	50	80	-	50	80	-	DCLK
Horizontal Address	THA	-	600	-	-	600	-	DCLK
Horizontal Front Porch	THF	20	60	-	20	60	-	DCLK
Vertical Frequency	-	-	60	-	-	60	-	Hz
Vertical Total ⁽²⁾	TVT	(3)	1944	2047	(3)	1624	2047	THT
Vertical Synchronization	TVS	(3)	2	-	(3)	2	-	THT
Vertical Back Porch	TVB	(3)	10	-	(3)	10	-	THT
Vertical Address	TVA	(3)	1920	-	(3)	1600	-	THT
Vertical Front Porch	TVF	(3)	14	-	(3)	14	-	THT

5. 可靠性实验测试(Reliability Test Conditions And Methods)

序号	试验项目	试验条件及方法	试验设备	检验项目	检验工具												
1	高温高湿(静、动态)试验	温度 $60^{\circ}\text{C} \pm 3^{\circ}\text{C}$, 湿度 $90\% \pm 3\%$, 要求选择时间分别为 96 小时, 静、动态(产品点亮)在室温下恢复 2 小时后进行外观, 显示功能全画面检查。	恒温恒湿试验机	检验外观、功能、抗腐蚀性	目视/ 测试架/ 客户样机/ 显微镜												
2	高、低温冲击试验	静态 -30°C (30 分钟) $\sim 80^{\circ}\text{C}$ (30 分钟) $\sim -30^{\circ}\text{C}$ (30 分钟), 24 个循环, 在室温下恢复 2 小时后进行外观, 显示功能全画面检查。	冷热冲击试验机	检验外观、功能													
3	高温贮存试验	常温 $70^{\circ}\text{C} \pm 3^{\circ}\text{C}$ 、宽温 $80^{\circ}\text{C} \pm 3^{\circ}\text{C}$ 、96 小时后在室温状态下恢复 1 小时在 2 小时内完成外观、显示功能全画面检查。	烤箱	检验外观、功能	目视/ 测试架/ 客户样机												
4	低温贮存试验	常温 $-20^{\circ}\text{C} \pm 3^{\circ}\text{C}$ 、宽温 $-30^{\circ}\text{C} \pm 3^{\circ}\text{C}$ 、条件的试验箱内保存 96 小时后在室温状态下恢复 1 小时, 在 2 小时完成外观、显示功能全画面检查, 特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。	低温冰箱	检验外观、功能	目视/ 测试架/ 客户样机												
5	低温贮存试验(动态)	常温 $-20^{\circ}\text{C} \pm 3^{\circ}\text{C}$ 、宽温 $-30^{\circ}\text{C} \pm 3^{\circ}\text{C}$ 条件的试验箱内点亮刷屏, 过程中每 1 小时观察一次, 全画面检查显示功能如: 异常, 卡机, 花屏等。特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。	低温冰箱	检验外观、功能	目视/ 测试架/ 客户样机												
6	包装模组跌落试验	<p>1、跌落重量及自由落体高度: (图二)</p>  <p>2、自由落体角度如下:</p> <table border="1" data-bbox="268 1545 646 1904"> <thead> <tr> <th>总重量</th> <th>自由落体高度</th> </tr> </thead> <tbody> <tr> <td>0-9kg</td> <td>92cm</td> </tr> <tr> <td>9-25kg</td> <td>76cm</td> </tr> <tr> <td>25-45kg</td> <td>53cm</td> </tr> <tr> <td>45-68kg</td> <td>46cm</td> </tr> <tr> <td>大于 68kg</td> <td>41cm</td> </tr> </tbody> </table> <p>3) 一角: A 角 2) 三菱: A-B, A-D, A-C 3) 六面: 面 1, 面 2, 面 3, 面 4, 面 5, 面 6;</p>	总重量	自由落体高度	0-9kg	92cm	9-25kg	76cm	25-45kg	53cm	45-68kg	46cm	大于 68kg	41cm	包装模组跌落架	测试电性能无异常、外观检验无破损, 无脱离现象	目视/ 测试架/ 客户样机
总重量	自由落体高度																
0-9kg	92cm																
9-25kg	76cm																
25-45kg	53cm																
45-68kg	46cm																
大于 68kg	41cm																

7	盐雾试验	<p>标准条件:中性盐雾试验(NSS 试验):5%的氯化钠盐水溶液,溶液 PH 值中性(6.5~7.2),试验温度 35±2℃,盐雾的沉降率在 1~2ml/80cm².h 之间,时间 24h。2.其它特殊要求条件:醋酸盐雾试验(ASS 试验):5%氯化钠溶液中配入冰醋酸,溶液 PH 值为 3 左右,试验温度 35±2℃,盐雾的沉降率在 1~2ml/80cm².h 之间,时间 24h。全画面检查外观、功能,特别注意检查是否有腐蚀</p>	盐雾试验设备	<p>检验外观、功能,盐雾试验结果的判定方法,腐蚀物出现判定法:定性判定,试验后功能测试应OK,外观观察产品无腐蚀现象产生。</p>	目视/测试架/客户样机/显微镜
8	ESD 防静电试验	<p>1)装整机状态下试验:接触 4KV,非接触 8KV 放电测试,接触测试时,LCM 通电状态下测 5 个点。 2)测试架测试状态下试验:接触 4KV,非接触 8KV 放电测试,接触测试时,LCM(或总成)通电状态下测 9 个点。其中产品正面显示区域两个点,产品显示区域背面 4 个点,产品左侧面、右侧面和 IC 端对面中间位置各一个点。(如 6.17.3.3 图所示)测试点 1—6 是空气放电,测试点 7—9 是接触放电,10 次/点。总成(或模组)实验后在图案、黑色、白色、灰阶画面各撕膜 3~5 次,确认有无撕膜静电不良,撕膜静电速度适中,不可过快及刻意放慢。判定标准:撕膜 3 次确认无撕膜静电 OK。撕膜 3 次以上出现撕膜静电,在保护膜覆盖后 3 秒内静电消失 OK。撕膜出现撕膜静电,在保护膜覆盖后 3 秒内静电不消失 NG。</p>	防静电枪(尖头接触放电,圆头空气放电)	检验外观、功能	目视/测试架

6. 光电参数 (Optical Characteristics)

6.1 光学规格 (Optical Specifications)

Parameter	Specification	Unit	Remarks
Active Area	107.64(H)*172.224(V)	mm	
Number Of Pixels	1200(H)×1920(V)	pixels	
Pixel Pitch	0.0299(H)×RGB×0.0897(V)	mm	
Pixel Arrangement	Pixels RGB stripe arrangement		
Display Mode	Normally Black		
Display Colors	16.7M(8bits)	colors	
Driver Inversion	Column		
Contrast Ratio	1000:1(typ.)		
Viewing Angle(CR>10)	85/85/85/85(typ.)	deg.	
Response Time	30(typ.), 35(max.)	ms	
Color Gamut	NTSC 87%		搭配RG LED

6.2 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit.

Parameter	Symbol	Min.	Max.	Unit	Remarks
LC operating Voltage [Note 2.1]	V _{OP}	4.2	4.6	V	Ta=25+/-5°C
Operating Temperature (Humidity)	T _{OP}	-20	+60	°C	
	RH(60°)		90	%	
Storage Temperature (Humidity)	T _{ST}	-30	+70	°C	
	RH(60°)		90	%	

Note 2.1: Liquid Crystal driving voltage: Due to the characteristics of LC Material, this voltage varies with environmental temperature.

7. 检验标准 (Inspection standard)

71 Inspection conditions is as follows

- 1) Viewing angle is within $\pm 30^\circ$ from vertical direction, as fig 1
- 2) Viewing angle is the angle defined in the drawing
- 3) Ambient temperature is approximately $25 \pm 5^\circ \text{C}$
- 4) Ambient luminance is about 300~500 Lux.

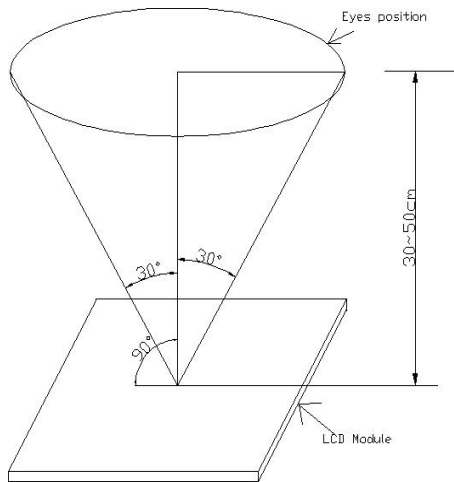
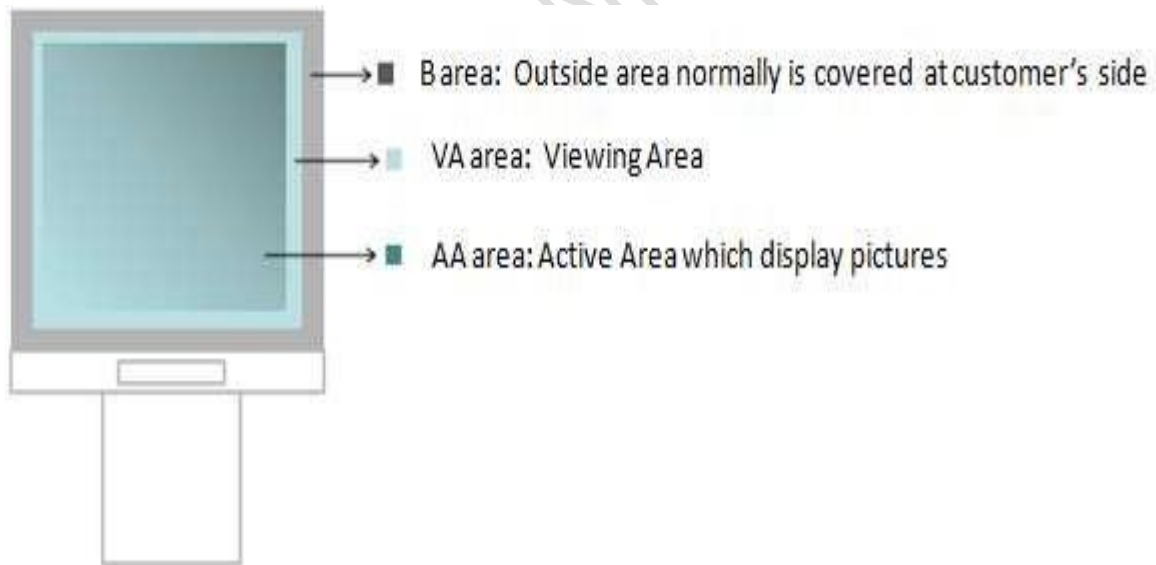


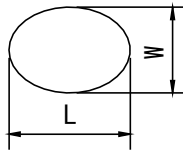

fig1

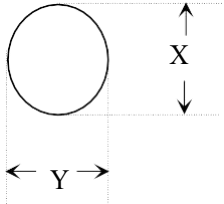
72 Panel area definition

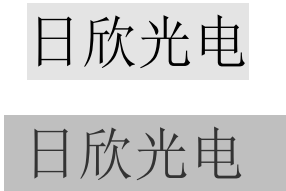
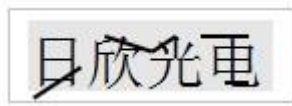


73 Routine inspection standards

7.3.1、外观检验标准:

项目	不良描述	判定标准				检验方法																					
1-1 外观 (次缺)	产品外观或点亮状态下的圆形物 (LCD/POL/BL/盖板/TP/组装异物/贴合异物、产品本身的亮点/暗点等)  $\Phi=(L+W)/2$	(7寸-≤12寸) : <table border="1"> <thead> <tr> <th>点状直径</th> <th>允收个数</th> <th colspan="2">备注</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.1$</td> <td>不计</td> <td colspan="2">两点间距 15mm</td> </tr> <tr> <td>$0.1 < \Phi \leq 0.2$</td> <td>2</td> <td colspan="2">两点间距 15mm</td> </tr> <tr> <td>$0.2 < \Phi \leq 0.3$</td> <td>1</td> <td colspan="2"></td> </tr> <tr> <td>$\Phi > 0.3$</td> <td>0</td> <td colspan="2"></td> </tr> </tbody> </table>				点状直径	允收个数	备注		$\Phi \leq 0.1$	不计	两点间距 15mm		$0.1 < \Phi \leq 0.2$	2	两点间距 15mm		$0.2 < \Phi \leq 0.3$	1			$\Phi > 0.3$	0			目视 (菲林卡比对)	
		点状直径	允收个数	备注																							
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1-2 外观 (次缺)	产品外观或点亮状态下的线状物 (LCD/POL/BL/盖板/TP/组装异物/贴合异物、产品本身的亮点/暗点等) 	(7寸-≤12寸) : <table border="1"> <thead> <tr> <th>L</th> <th>W</th> <th>允收个数</th> <th>备注</th> </tr> </thead> <tbody> <tr> <td>$L \leq 3$</td> <td>$W \leq 0.03$</td> <td>不计</td> <td>两线间距 15mm</td> </tr> <tr> <td>$L \leq 5$</td> <td>$0.03 < W \leq 0.05$</td> <td>2</td> <td>两线间距 15mm</td> </tr> <tr> <td>$L > 5$</td> <td>$W > 0.05$</td> <td>0</td> <td></td> </tr> </tbody> </table>				L	W	允收个数	备注	$L \leq 3$	$W \leq 0.03$	不计	两线间距 15mm	$L \leq 5$	$0.03 < W \leq 0.05$	2	两线间距 15mm	$L > 5$	$W > 0.05$	0		目视 (菲林卡比对)					
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1-4 外观 (次缺)	导电布、胶带贴附不良	1、ITO 点银浆位置贴附导电布贴偏超出 LCD 边缘 NG 2、导电布未连接上玻璃 NG 3、导电布贴附位置与图纸不符 NG 4、漏贴导电布、IC 防紫外线胶、FPC 保护胶 NG	目视																				
1-5 外观 (次缺)	焊接不良 1、A/K 点或 T/P 焊接点歪、锡量超厚、未焊接、虚焊、假焊。 2、A/K 点或 T/P 焊接点未清洁。 3、焊接线沾锡 4、T/P 焊接对位	1、A/K 焊点按搭接面积大于 2/3 OK, 焊点厚度不超过工程图上限, A/K 或 TP 焊点未焊接、虚焊、假焊 NG 2、A/K 点或 T/P 焊接点有残渣、松香油、脏污等 NG 3、FPC 焊接线有锡, 分开包装, 提示入库。 4、以焊接丝印线为基准, 下焊超过丝印 0.2mm NG。上焊与丝印靠齐距离大于 0.5mm NG.	目视 (必要时放大镜确认)																				

1-6 外观 (次缺)	FPC 弯折 1、FPC 边缘未与 BL 边缘平齐，压印线未与定位线对准。 2、元器件顶住背光胶框。	1 FPC 反折要用反折治具检查，未折到位，FPC 边缘须与 BL 边缘平齐，压印线定位孔未对准， NG； 2 用手指摸背光背面元件区域平整，目视元件有无顶住 BL 边缘，并且预留 0.2MM 间距 OK	卡尺测量
1-7 外观(次缺)	总成贴合偏位	总成贴合偏位（上下左右），按图纸要求进行管控，不可超出图纸管控范围，如超出则 NG	卡尺测量
7.3.2、电讯检验标准：			
项目	不良描述	判定标准	检验方法
2-1 电讯 (主缺)	漏液晶	LCD 因密封性受损导致空气进入液晶盒内 NG	目视，必要时投低温验证
2-2 电讯 (主缺)	少划： LCD 点亮后有整行(或列)或字段点阵不显的现象	OK 	用测架点亮 LCD 后目视
2-3 电讯 (主缺)	乱讯：在显示字体画面时有不该显示的地方显示(画面乱七八糟)	 NG	用测架点亮 LCD 后目视

2-4 电 讯 (主 缺)	字节不均(暗画): 需要显示的字节 本身有明暗不一致现象	 NG	用测架点 亮LCD 后目 视
2-5 电 讯 (主 缺)	多画: 有不需显示之字节出现在 显示区内	 NG	用测架点 亮LCD 后目 视
2-6 电 讯 (主 缺)	显示深浅: 比对样品有字深字淡现 象(在测试条件一致的情况下量测 产品 Vop 值是否在偏差范围内)	 深 标准 浅	必要时可 用主机板 确认
2-7 电 讯 (主 缺)	无显: 通电后 LCD 无动作或无画面	NG	用测架点 亮LCD 后目 视

8. 模组使用注意事项 (Precautions for Use of LCD Modules)

81 如果接口定义内有定义IM0, 请根据规格书(4.接口定义)内的定义做正确选择以匹配数据线的位数。

82 客户在做结构设计时, 请保证机壳开窗尺寸比触摸屏 V.A 单边少 0.3mm。泡棉开窗尺寸比触摸屏 V.A 单边大 0.2mm。

83 模组的主要部件LCD 和 TP 都是由玻璃组成, 在测试、使用、移动过程中, 请轻拿轻放。当产品不带触摸屏时, 靠近 FPC 的屏幕两端绝对不能受力, 否则会导致玻璃破损和显示不良的发生。

84 粘合偏光片、背光、触摸屏的胶材是有机物质, 在接触到甲苯、乙醇、丙酮时, 会破坏粘性。在使用中, 请防止这些物质接触到产品。

85 如果显示表面掉落有灰尘、异物, 切忌用手直接擦拭。请用棉签轻轻挑擦。

86 如果LCD 破损导致液晶泄露, 请不要让皮肤或衣服沾到液晶。如果不小心碰到, 请立即用

肥皂和清水清洗。

- 87 用手直接触摸显示区域会造成偏光片的损坏，同时容易引起静电问题。
- 88 当模组运行时，在显示区域施加压力会导致显示不正常。撤去外力，重新开机，可以恢复。
- 89 潮湿的环境可能引起玻璃ITO的腐蚀，在使用中，请确保湿度在 60%以下。

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